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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,461	03/30/2004	Vicki W. Tsai	80107.116US1	4678

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EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,461	TSAI ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/20/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is in response to application 10/813,461, amendment filed 11/20/2006. Claims 1, 5, 18, 24 and 28 are currently amended. Claim 4 is cancelled. Claims 1-3 and 5-30 are currently pending in this application.

1. Applicant's arguments filed 11/20/2006 have been fully considered but they are not persuasive. The applicable rejections from the prior office action have been incorporated herein, with respect to Applicant's amendments.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. **Claims 1-30 is rejected under 35 U.S.C. 102(a)** as being anticipated by Vandeweerd et al. (US PG Pub 2004/0006584).

4. With respect to claim 1, Vandeweerd teaches:

translating a design description into configurations for a plurality of processing elements (i.e. translate a specification of an integrated circuit into an implementation, paragraph [0002]), wherein a plurality of functions in the design description are implemented on one of the plurality of processing elements (i.e. at least some threads [functions] within one processing engine, see Abstract);

setting at least one output packet size corresponding to at least one of the plurality of functions (i.e. a decision can be made about the packet and message lengths, paragraph [0434]);

estimating network performance (i.e. performance estimates of design options, paragraph [0013]) (i.e. performance of the network, paragraph [0354]); and

modifying a clock frequency of at least one of the plurality of processing elements (reducing the clock frequency of the clock island's processor clock, paragraph [0385]).

5. With respect to claim 18, Vandeweerd teaches:

dividing a design description into a plurality of functions (i.e. implementing a multi-threaded technology with specified functionality using primitive design elements, paragraph [0016]);

mapping (i.e. descriptions can be mapped, paragraph [0040]) at least two of the plurality of functions (i.e. a first set of threads [functions or primitive elements], paragraph [0055]) onto one of a plurality of processing elements (i.e. within one processing engine, see Abstract) in an integrated circuit; setting a first output packet size for a first of the at least two of the plurality of functions (i.e. a decision can be made about the packet and message lengths, paragraph [0434]);

setting (packet length PL=4, paragraph [0416]) a second output packet size for a second of the at least two (a first set of threads [i.e. two or more functions], paragraph [0055]) of the plurality of functions (i.e. packets of a given packet length for several threads [functions] or processors, paragraph [0432]);

estimating network performance (i.e. performance estimates of design options, paragraph [0013]) (i.e. performance of the network, paragraph [0354]); and

modifying a clock frequency of at least one of the plurality of processing elements (reducing the clock frequency of the clock island's processor clock, paragraph [0385]).

6. With respect to claim 24, Vandeweerd teaches an apparatus including a medium to hold machine-accessible instructions (i.e. computer program product with computer readable program means, paragraph [0085]) that when accessed result in a machine performing:

reading a design description (i.e. Hardware specification as input, see Fig 1);

compiling (i.e. using a compiler, paragraph [0015]) the design description (i.e. multi-threaded description, paragraph [0034]) to configure a plurality of processing elements, wherein a plurality of functions in the design description are mapped to one of the plurality of processing elements (i.e. thread(s) in parallel on a single CPU, paragraph [0033]);

independently determining output packet sizes for each of the plurality of functions (i.e. a decision can be made about the packet and message lengths, paragraph [0434]); and

independently determining clock frequencies for each of the plurality of processing elements (reducing the clock frequency of the clock island's processor clock, wherein the processor clock is independent from the clock systems of other islands, paragraph [0385]).

7. With respect to claim 28, Vandeweerd teaches a system comprising:

a processor (i.e. one processing engine, paragraph [0055]);

a static random access memory to hold instructions that when accessed result in the processor performing translating a design description (i.e. translates these descriptions, paragraph [0054]) into configurations for a plurality of processing elements (i.e. a number of separate processors, paragraph [0055]) on a single integrated circuit (i.e. single chip implementation, paragraph [0055]), wherein a plurality of functions (at least some threads [i.e. functions], paragraph [0055]) in the design description are implemented on one of the plurality of processing elements (i.e. at least some of the processors executing a thread, paragraph [0055]), independently determining clock frequencies for each of the plurality of processing elements (reducing the clock frequency of the clock island's processor clock, wherein the processor clock is independent from the clock systems of other islands, paragraph [0385]), and setting at least one output packet size corresponding to at least one of the plurality of functions (i.e. a decision can be made about the packet and message lengths, paragraph [0434]).

8. With respect to claims 2 and 29, Vandeweerd teaches all the elements of claims 1 and 28, from which the claims depend respectively. Vandeweerd teaches: wherein setting at least one output packet size comprises setting independent output packet sizes for more than one of the plurality of functions (i.e. a decision can be made about the packet and message lengths, paragraph [0434]).

9. With respect to claims 3 and 30, Vandeweerd teaches all the elements of claims 1 and 29, from which the claims depend respectively. Vandeweerd teaches: wherein

setting at least one output packet size comprises setting an independent output packet size for each of the plurality of functions (i.e. a decision can be made about the packet and message lengths, paragraph [0434]).

10. With respect to claim 5, Vandeweerd teaches all the elements of claim 1, from which the claim depends. Vandeweerd teaches: modifying the at least one output packet size (i.e. change to a higher packet size, paragraph [0435]) and re-estimating network performance (i.e. performance is increased, paragraph [0453]) (i.e. if performance requirements are not met, changes are made, and simulation validates [re-estimates] performance, paragraph [0147]).

11. With respect to claim 6, Vandeweerd teaches all the elements of claim 1, from which the claim depends. Vandeweerd teaches: wherein translating comprises compiling the plurality of functions (RTL functions can be moved to threads [], wherein a thread performs a specific function [0070], a thread is a sequence of instructions [code], paragraph [0015]) to code to run on the one of the plurality of processing elements (i.e. a number of separate processors [0055]).

12. With respect to claim 7, Vandeweerd teaches all the elements of claim 1, from which the claim depends. Vandeweerd teaches: wherein setting a packet size comprises dividing a function output block size into smaller physical block sizes (i.e. the data stream is divided into blocks, paragraph [0302]).

13. With respect to claim 8, Vandeweerd teaches all the elements of claim 7, from which the claim depends. Vandeweerd teaches: wherein setting a packet size further

includes adding a packet header size to the physical block size (i.e. a packet consists of a header and data, paragraph [0345]).

14. With respect to claim 9, Vandeweerd teaches all the elements of claim 1, from which the claim depends. Vandeweerd teaches: profiling a design represented by the configurations for the plurality of processing elements (i.e. simulations on the network, paragraph [0421]).

15. With respect to claim 10, Vandeweerd teaches all the elements of claim 9, from which the claim depends. Vandeweerd teaches: changing the at least one output packet size in response to the profiling (i.e. change to a higher packet size, paragraph [0435]).

16. With respect to claim 11, Vandeweerd teaches all the elements of claim 9, from which the claim depends. Vandeweerd teaches: comparing user constraints (i.e. given performance constraints, paragraph [0147]) with output (i.e. simulations of latency and throughput, paragraphs [0128] and [0363]) from the profiling (i.e. performance requirements/parameters are considered, paragraph [0388]).

17. With respect to claim 12, Vandeweerd teaches all the elements of claim 11, from which the claim depends. Vandeweerd teaches: wherein the user constraints include latency (i.e. minimal latency, paragraph [0380]).

18. With respect to claim 13, Vandeweerd teaches all the elements of claim 11, from which the claim depends. Vandeweerd teaches: wherein the user constraints include throughput (i.e. maximum throughput, paragraph [0363]).

19. With respect to claim 14, Vandeweerd teaches all the elements of claim 1, from which the claim depends. Vandeweerd teaches: wherein each of the plurality of functions has an output block size (i.e. the data stream encoded is divided into blocks, paragraph [0302]), and wherein setting at least one output packet size comprises dividing the output block size to set a physical packet size (i.e. incoming bit stream [block] divided into frames, paragraph [0296]).

20. With respect to claim 15, Vandeweerd teaches all the elements of claim 14, from which the claim depends. Vandeweerd teaches: wherein setting at least one output packet size further comprises estimating network performance (i.e. determining latency of packets through simulations [0405], effectively resulting in determining network performance [0412]).

21. With respect to claim 16, Vandeweerd teaches all the elements of claim 15, from which the claim depends. Vandeweerd teaches: changing the physical packet size in response to the estimating (i.e. after a simulation is performed and latencies [performance] are determined, packet sizes can be determined [0434], changed [0435]).

22. With respect to claim 17, Vandeweerd teaches all the elements of claim 15, from which the claim depends. Vandeweerd teaches: wherein profiling produces information describing throughput (i.e. throughput, paragraph [0350]).

23. With respect to claim 19, Vandeweerd teaches all the elements of claim 18, from which the claim depends. Vandeweerd teaches: wherein the first of the at least two of the plurality of functions has an output block size (i.e. block sizes, paragraph [0302]),

and wherein the first output packet size is smaller than the output block size (i.e. a message block is segmented into packets, paragraph [0319]).

24. With respect to claim 20, Vandeweerd teaches all the elements of claim 18, from which the claim depends. Vandeweerd teaches: generating configuration packets to configure the integrated circuit (i.e. a message is segmented into packets, paragraph [0319]).

25. With respect to claim 21, Vandeweerd teaches all the elements of claim 20, from which the claim depends. Vandeweerd teaches: configuring the integrated circuit with the configuration packets (i.e. passing messages [packets] among nodes of the parallel computing system [integrated circuit], paragraph [0324]).

26. With respect to claim 22, Vandeweerd teaches all the elements of claim 20, from which the claim depends. Vandeweerd teaches: profiling a design with the configuration packets (i.e. determining message latency, paragraph [0344]).

27. With respect to claim 23, Vandeweerd teaches all the elements of claim 22, from which the claim depends. Vandeweerd teaches: modifying the first output packet sizes in response to the profiling (i.e. change to a higher packet size, paragraph [0435]).

28. With respect to claim 25, Vandeweerd teaches all the elements of claim 24, from which the claim depends. Vandeweerd teaches: estimating a performance (i.e. performance estimates, paragraph [0013]) of the plurality of processing elements; and modifying at least one of the output packet sizes in response to the estimating (i.e. change to a higher packet size, paragraph [0435]).

29. With respect to claim 26, Vandeweerd teaches all the elements of claim 25, from which the claim depends. Vandeweerd teaches: wherein estimating a performance (i.e. performance constraints, paragraph [0147]) comprises determining if throughput constraints are met (i.e. performance and throughput, paragraph [0363]).

30. With respect to claim 27, Vandeweerd teaches all the elements of claim 26, from which the claim depends. Vandeweerd teaches: wherein determining if throughput constraints are met comprises determining if throughput constraints (i.e. maximum throughput, paragraph [0363]) for each of the plurality of functions (functions, paragraph [0036]) are met.

Response to Arguments

31. Applicant's arguments filed 11/20/2006 have been fully considered but they are not persuasive. Examiner's response to arguments follows below.

32. Applicant asserts that Vandeweerd does not disclose, teach, or suggest "modifying a clock frequency of at least one of the plurality of processing elements". Examiner disagrees with this assertion.

33. Examiner points out that Vandeweerd teaches: modifying a clock frequency of at least one of the plurality of processing elements (reducing [i.e. modifying] the clock frequency of the clock island's processor clock [wherein the clock island controls the clock for at least one of possibly a plurality of processing elements], paragraph [0385]).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

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Suchin Parihar
Examiner
AU 2825

PAUL DINH
PRIMARY EXAMINER